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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PATEL, KAUSHIKKUMAR M	
ART UNIT	PAPER NUMBER
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/785,575	KACZYNSKI, TOMASZ	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/24/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on February 24, 2004 has considered by the examiner.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "112" in fig. 1 has been used to designate both memory unit and I/O interface. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1-6, 22-25, 28-31, 32-34 and 39-42 are objected to because of the following informalities:

Acronyms (such as ISDS in claim 1, or ISDC in claim 3) should not be used to abbreviate key terms or phrases until they are explicitly defined previously within the claim or a claim to which it depend.

With respect to claim 23, the term "system cache identifier" is not defined or disclosed in the specification, and examiner understood as "SELECT_CELL" field recited in claim 4 during this office action.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 35-42 are rejected under 35 USC 101, because claims are not limited to tangible embodiments. In view of applicants' disclosure, specification page 8, line 21 to page 9, line 3, the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g. ROM, RAM, magnetic/optical storage medium etc.) and intangible embodiments (e.g. electrical, optical propagated signals and carrier waves). As such, the claims are not limited to statutory subject matter and are therefore non-statutory.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 10-12, 18-21 and 35-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michael et al. (US 2002/0002659 A1) and further in view of Joseph et al. (US 6,405,292) and Carpenter et al. (US 6,266,743).

As per claim 1, Michael teaches a method comprising:

receving in an ingrained sharing directory cache (ISDC) an incoming operation request including an associated incoming memory address (Michael, pars. [0019], [0033], [0035], taught as receiving, in the directory cache, a disk or memory request, memory request inherently requires associated address);

performing the operation, if there is an ISDC entry associated with the incoming memory address (Michael, par. [0035], if there is a hit in the DC, the corresponding directory information is read); and

creating an ISDC entry if there is no ISDC entry associated with the incoming operation request (Michael, par. [0035], if a his is not detected, the requested information is acquired from the memory directory); wherein creation includes,

requesting information associated with the incoming memory address, wherein the information is requested from an ingrained sharing directory storage (ISDS) (Michael, par. [0035], if a hit is not detected, the requested information is acquired from the memory directory, par. [0036], teaches address);

evicting another ISDC entry if there is no free ISDC entry; wherein the eviction includes requesting the ISDS to store the information evicted from the other entry

(Michael, par. [0032], the information is written back into the memory directory, par. [0036], if none of the ways is invalid (i.e. no free entry), one of them is selected and its contents are written to the memory directory); designating the evicted ISDC entry to the incoming request (Michael, par. [0036], one entry is selected and its contents are written to the memory directory, and replaced by the new tag and the directory entries from the memory directory).

Michael fails to teach pending buffer as required by claim. Joseph teaches pending buffer used by coherent controllers (Joseph, col. 1, lines 21-67) and Carpenter teaches eviction of cache entry using pending buffer (Carpenter, col. 8, lines 28-55). Joseph and Carpenter both teach that pending buffers maintains the status of memory transactions in progress and means for detecting collisions if there is another request for same entry (Joseph, col. 1, lines 14-20, Carpenter, col. 8, lines 50-55). Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to use pending buffer as taught by Joseph and Carpenter in the system of Michael to maintain coherency while transaction is in state of transition avoiding collisions (Joseph, col. 1, lines 14-20, Carpenter, col. 8, lines 50-55).

With respect to remaining limitations, such as locating pending operation in the pending queue and making evicted entry pending, Joseph teaches putting a memory request in pending buffer during memory transaction in progress i.e. in case of directory cache miss in the system of Michael, the request is stored in the pending buffer while awaits the required information being acquired from the memory directory (Joseph, col. 1, lines 14-67). Carpenter teaches that selected eviction entry is placed in eviction

buffer (pending buffer) and generated proper interconnect transactions (getting information from memory directory. Michael teaches that if memory tag does not match (miss), the controller request necessary information from memory directory, Michael, par. [0036]). Replacing a cache line from memory directory is a memory transaction in progress and it would have been obvious to one having ordinary skill in the art at the time of the invention to put in eviction buffer (pending buffer) as taught by Carpenter to maintain the coherency. Checking status of pending entry with respect response is inherent in the system of Joseph and Carpenter.

As per claim 2, Carpenter teaches different kinds of memory lines states (Carpenter, col. 4, lines 30-35, col. 7, line 50-67).

As per claim 10, Michael, Joseph and Carpenter teaches directory cache (Michael, fig. 4) to store state information about recent copies of local memory blocks (Michael, par. [0008]), the directory cache to receive directory storage requests and create directory cache entries from information presented by the directory storage (explained with respect claim 1, above); and

a directory cache pending queue to store pending operations (Joseph and Carpenter teach this limitation as explained with respect to claim 1 above).

Claim 11 is rejected under same rationales as applied to claim 2 above.

As per claim 12, Michael teaches writing state information to memory directory (Michael, par. [0032] and retrieving information from directory (pars. [0035]-[0036]), which inherently teaches fetching or modifying state information.

Claims 18-20 are similar in scope with respect to claim 1 and hence rejected under same rationales as applied to claim 1.

As per claim 21, Michael teaches directory cache and memory directory with state information indicating which cache(s) has a copy of the memory line (Michael, par. [0002]), which inherently teaches how many (only one or more or none) copies of memory line is present in the system. With respect limitation, wherein the memory line is located at the memory address, is inherent in order to work system error free.

Claims 35-38 are similar in scope with respect to claims 18-21 above and hence rejected under same rationales as applied to claims 18-21 above.

8. Claims 3-5, 7, 9, 13-17, 22-24, 28-34 and 39-41 are rejected under **35 U.S.C. 103(a)** as being unpatentable over Michael et al. (US 2002/0002659 A1), Joseph et al. (US 6,405,292) and Carpenter et al. (US 6,266,743) and further in view of Joseph et al. (US 6,338,123) (Joseph-2 herein after).

As per claim 3, Michael, Joseph and Carpenter teach receiving a directory storage request; and selecting an entry in an ISDS (see rejection of claim 1 above).

Michael, Joseph and Carpenter fail to teach, dynamic full map of memory lines as required by claim 3. Joseph-2 teaches dynamic full map directory keeping track of local memory lines in remote caches (Joseph-2, col. 2, lines 17-49). It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize dynamic full map directory as taught by Joseph-2 in the system of Michael, Joseph and Carpenter to improve system performance with simple coherence protocol (Joseph-2,

col. 2, lines 12-15). Joseph-2 teaches multi-way dynamic full map directory, which maintains state information of local lines cached in remote caches by each way for each remote cache (Joseph-2, col. 3, lines 14-60).

With respect to remaining limitations of claim 3, such as the structure of directory storage corresponding to remote and local caches (number of buffer equals to number of cache sets in remote and local caches) as well as cache structure such as direct or associative or set-associative, number of sets of directory, number of entries per sets etc. are not explicitly taught by Michael, Joseph, Carpenter and Joseph-2, but such information is merely a matter of design choice and would have been obvious in the system of Michael, Joseph, Carpenter and Joseph-2. These limitations fail to define a patentably distinct invention over Michael, Joseph, Carpenter and Joseph-2, since both the invention as a whole directed to maintaining dynamic full map of local memory lines in caches in remote system caches.

As per claims 4 and 5, Michael teaches set-associative directory cache and respective request formation, including tag, set ID, offset and state of the memory line (Michael, figs. 5-6), thus depending upon the structures of cache and directories (as explained with respect to claim 3 above) it is inherent to include SELECT_CB field, SELECT_CELL field for selection of respective buffer and further respective cell from buffer.

As per claim 7, Michael teaches coherence controller controlling operations with respect to system caches and directory cache as well as memory directory. Directory cache stores the information about memory lines cached in system caches (Michael, fig.

3, par. [0031]). Joseph, Carpenter and Joseph-2 teach pending queue and dynamic full map directory as explained with respect to claims 1 and 3 above.

As per claim 9, Michael teaches caches having set-associative structure (Michael, par. [0033]).

Claims 13-16 recites limitations, including number of nodes in the system, each node having number of set-associative caches, a directory storage having number of buffers and each buffer having some number of cells and cells with directory entries. All the limitations above are rejected under same rationales as applied to claim 3 as design choice and would have been obvious in the system of Michael, Joseph, Carpenter and Joseph-2.

As per claim 17, Michael teaches main memory unit (Michael, fig. 3, item 330), which is a random access memory.

Claims 22-24, 28-34 and 39-41 are rejected under same rationales as applied to claims 3-5 as well as claims 1-2 and 10-12 above.

9. Claims 6, 8, 25-27 and 42 are rejected under **35 U.S.C. 103(a)** as being unpatentable over Michael et al. (US 2002/0002659 A1), Joseph et al. (US 6,405,292), Carpenter et al. (US 6,266,743) and Joseph et al. (US 6,338,123) (Joseph-2 herein after) as applied to claims 3, 7, 22 and 39 above and further in view of Lai (US 5,564,035).

As per claims 6, 8, 25 and 42, Michael, Joseph, Carpenter and Joseph-2 teach all the limitation of parent claims but fail to teach memory line residing only in one buffer

or combination of ISDC set and ISDS set combined includes all copies of memory lines cached at any point in time. Lai teaches concept of caches having non-inclusive configuration, which teaches limitation memory line residing only in one buffer or total of all sets includes all copies of memory lines at any point in time (Lai, col. 3, lines 24-35). It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize non-inclusive cache levels as taught by Lai in the system of Michael, Joseph, Carpenter and Joseph-2 to increase the efficiency of caches and thus reducing adjacent level cache sizes (Lai, col. 3, lines 1-20).

As per limitations of claims 26-27, Michael, Joseph, Carpenter and Joseph-2 teach directory cache to store the state information about a first set of memory lines (cached lines) and directory storage for second set of memory lines (not cached) as explained with respect to claims 1 and 7 above and Lai teaches a concept of non-inclusive caches, which teaches each set includes one copy of memory line which is not included in the other set and the total of all lines represents all the memory lines stored in the cache and directory storage. Thus, Michael, Joseph, Carpenter, Joseph-2 and Lai combined teach all the limitations of claims 26 and 27.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER

12/19/06